1 # QUADRATURE OSCILLATOR

2 ## BACKGROUND OF THE INVENTION

3 1. Field of the Invention

4 The present invention relates to a quadrature oscillator, in particular to an

5 oscillator for use in wireless communication devices having the advantages of

6 low phase noise and low power dissipation.

7 2. Description of Related Arts

8 A quadrature oscillator is an oscillator that outputs with four different

9 phases mutually separated by a quarter of a cycle, or 90 electrical degrees. This

10 type of oscillator is generally used in the transceiver circuit of communication

11 devices, such as cellular phones, wireless telephones, wireless networking

12 devices, and all short-range blue-tooth communication devices. The transceiver

13 circuits of these communication devices usually have a super heterodyne

14 architecture, requiring a high precision filter for image rejection. However, it is

15 difficult to produce transceiver ICs embedded with high precision filters.

16 Therefore, the usual practice is to have a high precision filter soldered onto the

17 transmitter circuit, thus posing a space constraint for circuit layout and making it

18 difficult to reduce the related production costs.

19 To solve the above problems, direct conversion or low IF transceiver

20 architecture is proposed to avoid the use of an image rejection filter. To support

21 the above two architectures, transceivers have to rely on the oscillator outputs

22 with precise phase quadrature. How to develop a high precision oscillator having

23 quadrature output has become an interesting topic for discussion in the industry.

24 The above quadrature oscillator can be built using any one of the three

1   methods mentioned below. The first method is to use two frequency dividers

2   operated out-of-phase to produce the quadrature phase outputs. The second

3   method is to use a conventional two-phase oscillator with a phase shifter such as

4   a poly-phase filter to produce quadrature phase outputs. The third method is to

5   use two cross-coupled two-phase oscillators, on which the present invention is

6   based. The cross coupling of two two-phase oscillators forms a quadrature

7   oscillator, as shown in Fig. 11, including:

8   two symmetrical oscillators (75) (76) being respectively connected by

9   transistor pairs (M1, M2) (M3, M4) in a positive feedback structure to produce

10   negative resistance;

11   two tank circuits (73) (74) being respectively connected to the above

12   oscillators (75) (76) to produce positive resistance offsetting the negative

13   resistance through the above oscillators (75) (76); and

14   two coupling circuits (71) (72) being respectively connected to the

15   oscillators (75) (76) to produce quadrature phase outputs.

16   Under the above-mentioned architecture, one of the two oscillators (75)

17   (76) has two outputs with phase shift of 0 and 180 electrical degrees, and the

18   other outputs with phase shift of 90 and 270 degrees.

19   Since the oscillation frequency of the oscillator largely depends on the

20   resonant frequency of the tank circuit and the parasitic capacitance in the active

21   circuit, and the output amplitude is dependent on the Q of the tank circuit and the

22   negative resistance in the active circuit, it is clear that the tank circuit plays an

23   important role in this type of oscillator. However, as the Q of the tank circuit is

24   largely determined by the manufacturing process of the semiconductor, designers

1   can do little to alter its value, but it is possible to change the active circuit to

2   improve the output characteristics of the oscillator using economical means.

3   For an oscillator, the characteristics of the active circuit can be analyzed

4   through its linear characteristics in steady state. The negative resistance

5   generated by per unit output current can be used as an indicator. In Fig. 11, the

6   quadrature oscillator is formed by two cross-coupled symmetrical oscillators.

7   Taking either one of the two for the present analysis will produce identical result.

8   Accordingly, the small signal conductance of the oscillator at point V0 can be

9   represented by:

10   $$G_2 = -g_{m1} + \frac{g_{l1}g_{l3} + g_{l1}g_{m1}}{g_{m3} + g_{mb3} + g_{l1} + g_{l3}}$$

11   where

12   g_m represents the transistor gate-to-source transconductance,

13   g_l represents the small signal conductance across the drain and source,

14   and

15   g_{mb} represents the transistor bulk-to-source transconductance.

16   From the above-mentioned architecture of the quadrature oscillator, it is

17   clear that the source terminals of transistor pairs (M5, M6) (M7, M8) in the

18   coupling circuits (71) (72) are respectively connected in series to the drain

19   terminals of transistor pairs (M1, M2) (M3, M4) in the two oscillators (75) (76).

20   At the steady state operating point, the four output terminals are at the same

21   potential $V_0 = V_{180} = V_{90} = V_{270}$. For the transistor M1, the potential across its

22   drain and source terminals is equal to $V_{DS1} = V_{270} - V_{TH5}$, which is lower than

23   the potential across the gate and source terminals, that means the transistor M1 is

24   affected by the coupling transistor M5, causing the operating points of transistor

1 M1 to shift toward the linear region and resulting in the decrease of

2 transconductance (g_m).

3 Under the pre-condition not to increase the operating current, it is

4 necessary to increase the length/width of coupling transistor M5 such that the

5 physical appearance of transistor M5 will be considerably larger than oscillator

6 transistor M1, but this can cause proportional increase in parasitic capacitance

7 that will decrease the oscillation frequency and the tunable frequency range.

8 From the foregoing, it is found that the operating point of the transistors

9 in the conventional quadrature oscillator is seriously affected by the coupling

10 transistors to shift toward the linear region, causing degradation of the signal

11 conductance and the operating characteristics of the quadrature oscillator.

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13 SUMMARY OF THE INVENTION

14 The main object of the present invention is to provide an oscillator that

15 can effectively prevent shifting of the operating point of the oscillator toward the

16 linear region in order to boost transistor transconductance, without degrading the

17 oscillation frequency and the amplitude of the quadrature oscillator.

18 To this end, the architecture of the quadrature oscillator in accordance

19 with the present invention comprises:

20 two symmetrical oscillators being connected by two cross-coupled

21 transistors in a positive feedback structure to produce negative resistance;

22 two LC circuits being respectively connected to the above oscillators to

23 produce positive resistance offsetting the negative resistance through the above

24 oscillators; and

1   two coupling circuits being coupled to the above oscillators in order to

2   produce outputs with phase quadrature.

3   The two coupling circuits are each formed by two identical transistors,

4   where the drain terminals of the transistors are respectively connected to the

5   source terminals of the oscillators, such that the operating point of the oscillator

6   transistor is not affected by the coupling circuit and continues to work in the

7   saturation region, thus reducing phase noise and maintaining the operating

8   current with low power dissipation.

9   The features and structure of the present invention will be more clearly

10   understood when taken in conjunction with the accompanying drawings.

11   BRIEF DESCRIPTION OF THE DRAWINGS

12   Fig. 1 is a schematic circuit in accordance with the first preferred

13   embodiment of the invention;

14   Fig. 2 is a comparative diagram of the characteristic curves of negative

15   conductance in relation to different operation frequencies using the first preferred

16   embodiment;

17   Fig. 3 is a schematic diagram of the circuit in the quadrature oscillator in

18   accordance with the second preferred embodiment of the invention;

19   Fig. 4 is a comparative diagram of the characteristic curves of oscillation

20   frequency in relation to different control voltages using the second preferred

21   embodiment;

22   Fig. 5 is a comparative diagram of the characteristic curves of output

23   amplitude in relation to different operation frequencies using the second

24   preferred embodiment;

1   Fig. 6 is a comparative diagram of the characteristic curves of phase

2   noise in relation to different operation frequencies using the second preferred

3   embodiment;

4   Fig. 7 is a schematic diagram of the circuit in the quadrature oscillator in

5   accordance with the third embodiment of the invention;

6   Fig. 8 is a comparative diagram of the characteristic curves of oscillation

7   frequency in relation to different control voltages using the third preferred

8   embodiment;

9   Fig. 9 is a comparative diagram of the characteristic curves of output

10   amplitude in relation to different operation frequencies using the third preferred

11   embodiment;

12   Fig. 10 is a comparative diagram of the characteristic curves of phase

13   noise in relation to different operation frequencies using the third embodiment;

14   and

15   Fig. 11 is a schematic diagram of the circuit in a conventional quadrature

16   oscillator.

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18   DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

19   The present invention provides a preferred embodiment as shown in Fig.

20   1, comprising:

21   two symmetrical oscillators (11) (12) being formed by cross-coupled

22   transistor pairs (M1, M2) (M3, M4) in a positive feedback structure to produce

23   negative resistance;

24   two LC circuits (13) (14), wherein the outputs are respectively connected

1   to the oscillators (11) (12) in series to produce positive resistance offsetting the

2   negative resistance through the oscillators (11) (12);

3   two coupling circuits (15) (16) that are formed by transistor pairs (M5,

4   M6), (M7, M8), whereby

5   the transistors pairs (M5, M6), (M7, M8) are respectively connected in

6   series with corresponding transistor pairs (M1, M2) (M3, M4) of the two

7   oscillators (11) (12) and share the same current sources;

8   the transistor pairs (M5, M6), (M7, M8) have constant current sources

9   (17) (18);

10   the gate terminals of the transistor pairs (M5, M6) (M7, M8) in the

11   coupling circuits (15) (16) are cross-coupled to the output of the LC circuits (13)

12   (14) to produce outputs with four phase angles (V0, V180, V270, V90); and

13   the drain terminals of the transistor pairs (M5, M6) (M7, M8) in the

14   coupling circuits (15) (16) are respectively connected in series to the source

15   terminals of the transistor pairs (M1, M2) (M3, M4) in the oscillators (11) (12).

16   Under the above architecture, the small signal conductance at point V0

17   can be expressed as

18
$$G_1 = (g_{m1} - g_{l1})\left[\frac{-g_{l3}}{g_{m1} + g_{mb1} + g_{l1} + g_{l3}}\right],$$

19   where

20   g_m represents transistor gate-to-source transconductance,

21   g_l represents the small signal conductance across the drain and source

22   terminals, and

23   g_{mb} represents the transistor bulk-to-source transconductance.

1   From the above formula, it can be demonstrated that the quadrature

2   oscillator in accordance with the present invention possesses greater negative

3   conductance for small signals G_2 as compared with conventional oscillators.

4    $$G_2 = -g_{m1} + \frac{g_{l1}g_{l3} + g_{l1}g_{m1}}{g_{m3} + g_{mb3} + g_{l1} + g_{l3}}$$

5   This point can be demonstrated by simulation of the circuit action using

6   selected parameters. It is assumed that the shunt current through the quadrature

7   oscillator in the first embodiment in Fig. 11 is 15 mA; the width/length of the

8   transistor in the circuit are 50 μ m/0.35 μ m; and the operating voltage is 3V. The

9   characteristic curve for negative conductance in relation to different operation

10   frequencies is shown in Fig. 2, where the curve denoted by square dots represents

11   the relationship between the negative conductance and frequency in the present

12   invention, and the curve denoted by triangular dots represents the negative

13   conductance and frequency demonstrated for the conventional quadrature

14   oscillators. From the comparison of these two characteristic curves, it is therefore

15   clear that the quadrature oscillator in the present invention possesses greater

16   negative conductance. By allowing the oscillator transistors (M1, M2) (M3, M4)

17   to be operated in the saturation region, the phase noise can be maintained to a

18   minimum level. By creating the quadrature oscillator with a small circuit area,

19   chip designers are left with more freedom to optimize the circuit design of the

20   quadrature oscillator.

21   Another preferred embodiment of the invention is shown in Fig. 3. With

22   . the same basic architecture as the previous example, in the second embodiment

23   n-channel MOSFET is employed for the constant current sources (17) (18), and

24   LC circuits (13)(14) are formed by symmetrical inductor pairs (L1, L2) (L3, L4)

1 and varactor pairs (C1, C2) (C3, C4), wherein the varactor pairs (C1, C2) (C3, C4)

2 are formed by MOSFET transistors. The circuit action using the foregoing

3 architecture is simulated in Fig. 4, in which the characteristic curve in the present

4 invention is denoted by square dots, as compared with the characteristics curve

5 for the conventional oscillator is denoted by square dots. To compare the circuit

6 performance, both conventional oscillator and the present invention use the same

7 current sources and varactors setup with the same frequency range 2.33–

8 2.67GHz. The output amplitude and phase noise distribution for different output

9 frequencies are respectively shown in Figs. 5, 6. It is found that the output

10 amplitude in the present invention is 30% larger as compared with the

11 conventional quadrature oscillators, and the phase noise is lower by 2-4dB.

12   Still another embodiment of the quadrature oscillator is shown in Fig. 7,

13 in which the constant current sources (17) (18) are implemented by p-channel

14 MOSFET, whilst other components are similar to the previous example. In Fig. 8,

15 using this oscillator architecture to simulate the circuit action, the characteristics

16 curve (oscillation frequency versus control voltage) in the present invention is

17 denoted by square dots, and the characteristics curve for the conventional

18 oscillator is denoted by triangular dots. Both conventional oscillator and the

19 present invention use the same current sources and varactor setup with the same

20 frequency range 2.37– 2.55GHz. The output amplitude and phase noise

21 distribution curves for different output frequencies are respectively shown in

22 Figs. 9, 10. The output amplitude in the present invention is considerably larger

23 than in the conventional quadrature oscillators, and the phase noise is

24 considerably lower.

1   In summary, the quadrature oscillator in the present invention has the

2   advantages of larger amplitude and lower phase noise as compared with the

3   conventional oscillator, whereby the output terminal does not need any extra

4   amplifier, thus simplifying the circuitry which accordingly has a low power

5   consumption, and boosting the signal to noise ratio to prevent noise interference.

6   The quadrature oscillator in the present invention provides quadrature

7   phase outputs, suitable for application in wireless communication with low phase

8   noise and low power dissipation. In addition, the present invention also gives

9   circuit designers freedom for optimizing the oscillation frequency and frequency

10   range.

11   The foregoing description of the preferred embodiments of the present

12   invention is intended to be illustrative only and, under no circumstances, should

13   the scope of the present invention be so restricted.